

FORM-PTO-1390
(Rev. 10-98)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER

**TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371**

032326-072

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.8)

Unassigned

09/646564

INTERNATIONAL APPLICATION NO.
PCT/FR99/00583INTERNATIONAL FILING DATE
16 March 1999PRIORITY DATE CLAIMED
20 March 1998

TITLE OF INVENTION


DEVICES FOR HIDING OPERATIONS PERFORMED IN A MICROPROCESSOR CARD

APPLICANT(S) FOR DO/EO/US

Nathalie FEYT, Olivier BENOIT and David NACCACHE

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
 2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
 3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and the PCT Articles 22 and 39(1).
 4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
 5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☒ has been transmitted by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
 6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
 7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
 - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. ☐ have been transmitted by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☒ have not been made and will not be made.
 8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
 9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
 10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).
- Items 11. to 16. below concern other document(s) or information included:**
11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
 12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
 13. ☒ A FIRST preliminary amendment.
 - ☐ A SECOND or SUBSEQUENT preliminary amendment.
 14. ☐ A substitute specification.
 15. ☐ A change of power of attorney and/or address letter.
 16. ☐ Other items or information:

U.S. APPLICATION NO. (If known, Rec'd 37 C.F.R. 1.501) Unassigned 09/646564		INTERNATIONAL APPLICATION NO. PCT/FR99/00583		ATTORNEY'S DOCKET NUMBER 032326-072	
17. <input checked="" type="checkbox"/> The following fees are submitted:				CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO \$840.00 (970) International preliminary examination fee paid to USPTO (37 CFR 1.482) \$670.00 (956) No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) \$690.00 (958) Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$970.00 (960) International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) \$96.00 (962)					
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$ 840.00	
Surcharge of \$130.00 (154) for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492(e)).				\$ -0-	
Claims	Number Filed	Number Extra	Rate		
Total Claims	9 - 20 =	-0-	X \$18.00 (966)	\$ -0-	
Independent Claims	2 - 3 =	-0-	X \$78.00 (964)	\$ -0-	
Multiple dependent claim(s) (if applicable)			+ \$260.00 (968)	\$ -0-	
TOTAL OF ABOVE CALCULATIONS =				\$ 840.00	
Reduction for 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				\$ -0-	
SUBTOTAL =				\$ 840.00	
Processing fee of \$130.00 (156) for furnishing the English translation later than months from the earliest claimed priority date (37 CFR 1.492(f)).				\$ -0-	
TOTAL NATIONAL FEE =				\$ 840.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 (581) per property +				\$ -0-	
TOTAL FEES ENCLOSED =				\$ 840.00	
				Amount to be: refunded \$	
				charged \$	
a. <input checked="" type="checkbox"/> A check in the amount of \$ <u>840.00</u> to cover the above fees is enclosed. b. <input type="checkbox"/> Please charge my Deposit Account No. <u>02-4800</u> in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>02-4800</u> . A duplicate copy of this sheet is enclosed.					
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO:					
James A. LaBarre BURNS, DOANE, SWECKER & MATHIS, L.L.P. P.O. Box 1404 Alexandria, Virginia 22313-1404					
 SIGNATURE				James A. LaBarre NAME	
28,632				REGISTRATION NUMBER	

Patent
Attorney's Docket No. 032326-072

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Nathalie FEYT et al) Group Art Unit: Unassigned
Application No.: Unassigned) Examiner: Unassigned
Filed:)
For: DEVICES FOR HIDING)
OPERATIONS PERFORMED IN A)
MICROPROCESSOR CARD)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination and the calculation of filing fees, kindly amend the above-identified application as follows.

IN THE SPECIFICATION:

Page 1, following the title, insert the following:

--This disclosure is based upon, and claims priority from, French Patent Application No. 98/03471 filed March 20, 1998, and International Application No. PCT/FR99/00583, filed March 16, 1999, the contents of which are incorporated herein by reference.

Background of the Invention--;

Page 1, penultimate line, change "An" to --A--.

Page 2, line 26, change "other" to --others--;

between lines 28 and 29, insert the following heading:

--Summary of the Invention--.

Page 3, between lines 22 and 23, insert the following heading:

--Brief Description of the Drawings--.

Page 4, between lines 4 and 5, insert the following heading:

--Detailed Description--;

Page 4, line 15, change "earth" to --ground--.

IN THE CLAIMS:

1. (Amended) A device for hiding [the] operations performed by a component intended to be integrated into a smart card, [characterised in that it comprises] comprising at least one means [(20, 30, 28, 26)] for modifying [the] electrical current consumption of [the] said component during the performance of [the] said operations.

2. (Amended) A device according to Claim 1, [characterised in that the] wherein said means for modifying the current consumption comprises at least one circuit

[(30)] for integrating the current of the component so as to average the variations in this current over time.

3. (Amended) A device according to Claim 1, [characterised in that the] wherein said means for modifying the current consumption comprises at least one random signal generator [(28)] and an array of resistors [(20)], the power supply to each of the resistors being controlled by the random signals.

4. (Amended) A device according to Claim 1, [characterised in that it comprises] comprising a plurality of means [(20, 20₁, 30, 30₁)] for modifying the current consumption.

5. (Amended) A device according to Claim 1, [characterised in that the] wherein said component comprises an EEPROM memory, and said means for modifying the current consumption of the component [in the case of a memory (14) of the EEPROM type, consists in simultaneously performing:

-] performs an operation of writing to or erasing the memory [(14), referred to as a hiding operation, and

-] simultaneous with an operation of [the] a microprocessor in said smart card.

6. (Amended) A device according to Claim 5, [characterised in that, in order to implement a hiding writing operation, the memory (14) comprises a part (26)] wherein a portion of said memory is dedicated to the recording of a random data item.

7. (Amended) A device according to [one of Claims 1 to 5, characterised in that] claim 1 wherein the activation of the means of modifying the current consumption is controlled by [the] a microprocessor [(12)] so as to be activated solely for the operations to be protected.

8. (Amended) A device according to Claim 5, [characterised in that the] wherein said microprocessor [(12)] performs [at least the] a cryptographic calculation according to the following steps:

- starting of [the] a charge pump,
- presentation of a random data item on [the] a data bus,
- presentation of a writing address on [the] an address bus,
- initiation of [the] programming,
- performing the cryptographic calculation,
- stopping the programming, and
- stopping the charge pump,

so as to mask the footprint of the current consumption occasioned by [the] said cryptographic calculation.

9. (Amended) A method for hiding [the] operations performed by a component, [characterised in that it includes] comprising the following steps:

- starting of [the] a charge pump,
- presentation of a random data item on [the] a data bus,
- presentation of a writing address on [the] an address bus,
- initiation of [the] programming,
- performing [the] a cryptographic calculation,
- stopping the programming, and
- stopping the charge pump.


REMARKS

Entry of the foregoing amendments is respectfully requested. These amendments are intended to eliminate the multiple dependency of the claims.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____


James A. LaBarre
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(703) 836-6620

Date:

DEVICES FOR HIDING THE OPERATIONS PERFORMED IN A
MICROPROCESSOR CARD

The invention relates to microprocessor cards
5 and, in such cards, different devices for hiding the
operations performed in the card for the purpose of
improving security against fraudulent intrusions.

Chip cards are divided into several categories,
namely:

- ```

10 - simple-memory cards,
- - memory cards known as smart cards, and
 - microprocessor cards.

```

A simple-memory card makes it possible to perform read and write operations freely in the electrically erasable read only memory area. Such a card is inexpensive but does not offer sufficient security so that it is being used less and less.

An smart memory card notably improves the security of the read/write operations by enabling them



only when certain conditions implemented in hard-wired form are fulfilled.

5 A card in the third category contains a microprocessor capable of executing programs recorded in a memory and thus making calculations with secret data inaccessible to the world external to the card. Thus a key recorded in the memory can serve to validate an electronic transaction such as a purchase or a door opening without having to be manipulated outside the card.

10 Unfortunately, certain microprocessors have current consumptions which depend on the calculations made inside the card. Thus a cryptographic calculation comprising a calculation tree which depends on the digits of the key used will have different current consumption footprints according to the value of the key used. As a result a fraudster could correlate the current consumption footprint of the key used and thus go back to the value of the key.

20 To prevent this correlation, a usual countermeasure consists of programming the cryptographic algorithm so that, whatever the value of the key, the algorithm will always pass through the same calculation steps.

25 Many so-called "byte oriented" algorithms lend themselves well to this program mode, but other pose a few technical problems which are surmountable only at the cost of a less optimal calculatory performance.

30 The purpose of the present invention is therefore to use, in microprocessor cards, devices for hiding the

operations performed whilst permitting the programmer the free choice of the programming rules, whether or not they are of the "byte oriented" type.

5 This purpose is achieved by modifying or scrambling the consumption of the card so that its footprint is independent of the calculations made.

This modification or scrambling of the footprint can be obtained by adding a device to the card which modifies the current consumption.

10 In a first example embodiment, this device consumes electrical power in an irregular or random manner, which is added to that of the normal consumption.

15 In a second example embodiment, this device achieves a mean consumption by effecting, for example, an integration of the current consumed.

20 In a third example embodiment, this device triggers the microprocessor memory erasure or programming circuit which consumes power in a chaotic manner, power which masks the consumption due to the operations performed by the microprocessor during the programming or erasure of the memory.

25 Other characteristics and advantages of the present invention will emerge from a reading of the following description of particular example embodiments, the said description being given in relation to the accompanying drawings, in which:

- Figure 1 is a functional diagram of a first example embodiment of the invention,

- Figure 2 is a functional diagram of a second example embodiment of the invention, and

- Figure 3 is a functional diagram of a third example embodiment of the invention.

5 In the figures, which each show schematically different means for implementing the invention, the electronic chip 10 containing the microprocessor of the card comprises a central unit 12 and at least one memory 14, for example of the type known by the English  
10 acronym EEPROM, standing for Electrically Erasable Programmable Read Only Memory. This electronic chip has several input and/or output terminals  $16_1$  to  $16_s$ , one of which, referenced  $16_1$ , is connected to an electrical circuit 18 supplying voltage  $V_{CC}$  whilst the  
15 one referenced  $16_s$  is connected to earth.

The supply circuit 18 supplies the different elements of the electronic chip 10 with a current  $I_{out}$  and, notably, the memory 14 and the central unit 12. This current  $I_{out}$  varies according to the operations  
20 performed by the central unit and the memory and therefore reflects the cryptographic calculations, which could make it possible to determine the key thereof.

So that this current  $I_{out}$  no longer reflects the  
25 operations performed, the invention proposes to modify it by means of a device 20 or 30, disposed in the chip 10 and connected, for example, to the input terminal  $16_1$ .

The invention proposes to modify the current in  
30 two different ways. A first by ensuring that the

device 20 (Figure 1) consumes current in a random or at the very least irregular manner, random additional consumption which, added to the normal current consumption  $I_{in}$ , makes the value  $I_{out}$  random.

5       The second way consists in averaging the value of  $I_{in}$ , which does not make it possible to detect the variations in  $I_{in}$  due to the operations performed.

10       In the first case, the device 20 can be produced by means of resistors 30, in fact transistors, which are powered or not according to the random signals supplied by a generator 28. The currents flowing in the powered resistors increase, modifying the total current value and hiding the current due to the cryptographic calculations.

15       In the second case, the average of the current  $I_{in}$  is obtained by an integrator which "smooths" the variations in the current  $I_{in}$  so as to erase them.

20       According to the invention, several devices 20 or 30, referenced 20<sub>1</sub> and 30<sub>1</sub>, can be connected to different points on the electronic chip, for example to the power supply conductor of the central unit (reference 22). In addition, these devices 20, 20<sub>1</sub>, 30 and 30<sub>1</sub> can be connected or not, depending on whether the operations are to be protected or not, the connections being made under the control of signals  
25       supplied by the central unit 12 (broken lines).

30       The invention proposes a third way of scrambling the value of  $I_{out}$  whilst performing operations to be protected, such as cryptographic calculations, during certain phases of the operations of programming or

erasing the memory 14, these operations being under the control of the central unit 12.

This third way is based on the use of a memory 14 of the EEPROM type which has auto-writing capability.

5        In a normal operating mode, the microprocessor activates a programming circuit 24 of the memory 14 according to the following steps:

- 1 - activation of the charge pump,
- 2 - presentation, on the data bus, of the data  
10 item to be written,
- 3 - presentation on the address bus of the writing address,
- 4 - initiation of the programming,
- 5 - waiting during the programming time,
- 15 6 - stopping the programming,
- 7 - stopping the charge pump.

Since the programming of an EEPROM cell makes it necessary to inject electrical charges into the programmed cell, steps 4, 5 and 6 are accompanied by an  
20 over-consumption of current of chaotic appearance which depends essentially on the value of  $V_{CC}$ , the address, the programmed value and the temperature of the component.

25        In order to mask the current consumption footprint of a cryptographic calculation for example, the invention proposes to use the chaotic consumption of steps 4, 5 and 6 by performing the cryptographic calculation during step 5 for a period of a few microseconds.

To do this, the cryptographic calculation is performed according to the following steps:

- 1 - starting the charge pump,
- 2 - presentation of a random data item on the data bus,
- 3 - presentation of a writing address on the address bus,
- 4 - initiation of the programming,
- 5 - effecting the cryptographic calculation,
- 6 - stopping the programming,
- 7 - stopping the charge pump.

Through these steps, the footprint of the current consumption due to the cryptographic calculation of step 5 is masked by the writing of the random data item in a given part 26 of the EEPROM memory reserved for this function.

Instead of a cryptographic calculation, step 5 can consist of any operation to be protected vis-à-vis the outside.

In addition, instead of performing these operations to be protected during a writing in the memory 14, they can be done during an erasure of the memory 14.

## CLAIMS

1. A device for hiding the operations performed by a component intended to be integrated into a smart card, characterised in that it comprises at least one means (20, 30, 28, 26) for modifying the current consumption of the said component during the performance of the said operations.

2. A device according to Claim 1, characterised in that the means for modifying the current consumption comprises at least one circuit (30) for integrating the current of the component so as to average the variations in this current over time.

3. A device according to Claim 1, characterised in that the means for modifying the current consumption comprises at least one random signal generator (28) and an array of resistors (20), the power supply to each of the resistors being controlled by the random signals.

4. A device according to Claim 1, characterised in that it comprises a plurality of means (20, 20<sub>1</sub>, 30, 30<sub>1</sub>) for modifying the current consumption.

5. A device according to Claim 1, characterised in that the means for modifying the current consumption of the component in the case of a memory (14) of the EEPROM type, consists in simultaneously performing:

- an operation of writing to or erasing the memory (14), referred to as a hiding operation, and
- an operation of the microprocessor.

6. A device according to Claim 5, characterised in that, in order to implement a hiding writing

operation, the memory (14) comprises a part (26) dedicated to the recording of a random data item.

5 7. A device according to one of Claims 1 to 5, characterised in that the activation of the means of modifying the current consumption is controlled by the microprocessor (12) so as to be activated solely for the operations to be protected.

10 8. A device according to Claim 5, characterised in that the microprocessor (12) performs at least the cryptographic calculation according to the following steps:

15 - starting of the charge pump,  
- presentation of a random data item on the data bus,  
- presentation of a writing address on the address bus,  
- initiation of the programming,  
- performing the cryptographic calculation,  
- stopping the programming,  
20 - stopping the charge pump,  
so as to mask the footprint of the current consumption occasioned by the said cryptographic calculation.

25 9. A method for hiding the operations performed by a component, characterised in that it includes the following steps:

- starting of the charge pump,  
- presentation of a random data item on the data bus,



- presentation of a writing address on the address bus,

- initiation of the programming,
- performing the cryptographic calculation,
- stopping the programming,
- stopping the charge pump.

5

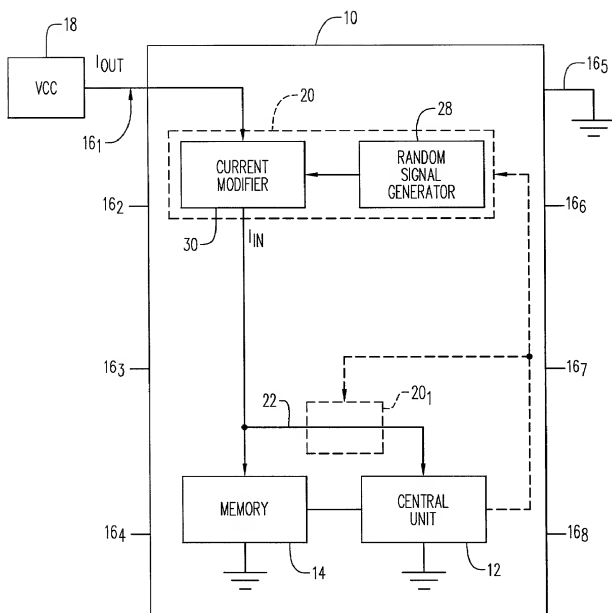


FIG. 1

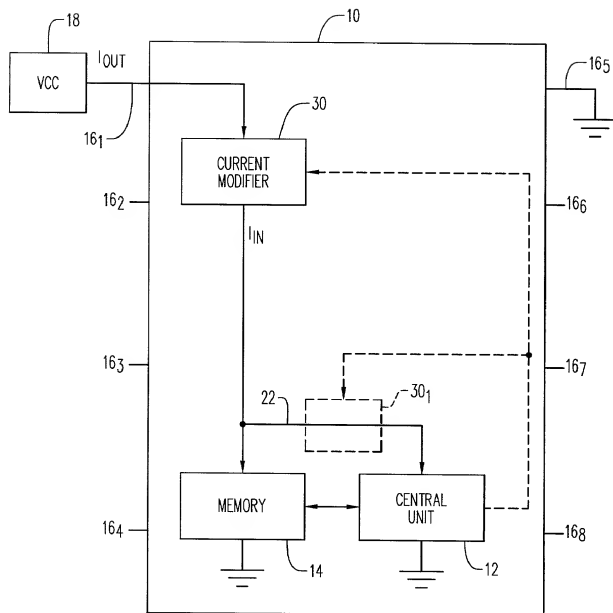


FIG. 2

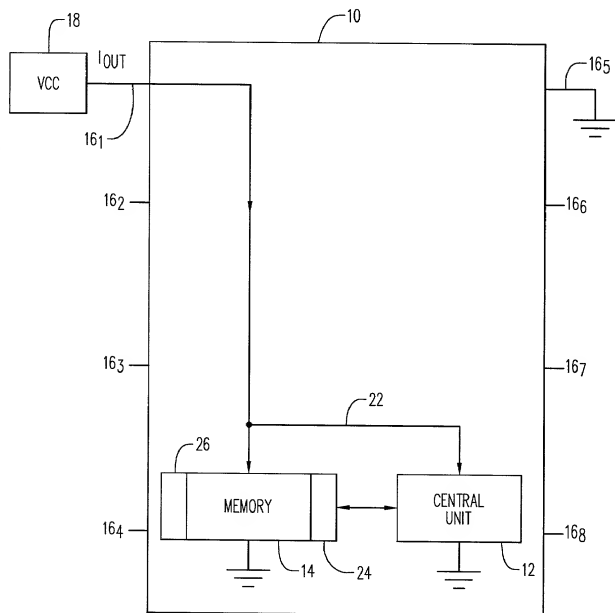


FIG. 3

**COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY**  
(Includes Reference to Provisional and International (PCT) Applications)

Attorney's Docket No.  
032326-072

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (IF ONLY ONE NAME IS LISTED BELOW) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (IF PLURAL NAMES ARE LISTED BELOW) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

DEVICES FOR HIDING OPERATIONS PERFORMED IN A MICROPROCESSOR CARD

The specification of which (check only one item below):

☐ is attached hereto.  
☒ was filed as United States Patent Application Number \_\_\_\_\_  
on September 20, 2000

and was amended on \_\_\_\_\_

(if applicable).

☐ was filed as International (PCT) Application Number \_\_\_\_\_  
on \_\_\_\_\_  
and was amended on \_\_\_\_\_

(if applicable).



I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE.

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE U.S. PATENT AND TRADEMARK OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than six months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code, §§ 119 (a)-(e) of any foreign application(s) for patent or inventor's certificate or of any International (PCT) Application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International (PCT) Application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

**PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119:**

| COUNTRY<br>(if PCT, indicate "PCT") | APPLICATION NUMBER | DATE OF FILING<br>(day, month, year) | PRIORITY CLAIMED<br>UNDER 35 U.S.C. §119                            |
|-------------------------------------|--------------------|--------------------------------------|---------------------------------------------------------------------|
| France                              | 98/03471           | 20 March 1998                        | <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No |
|                                     |                    |                                      | <input type="checkbox"/> Yes <input type="checkbox"/> No            |
|                                     |                    |                                      | <input type="checkbox"/> Yes <input type="checkbox"/> No            |
|                                     |                    |                                      | <input type="checkbox"/> Yes <input type="checkbox"/> No            |
|                                     |                    |                                      | <input type="checkbox"/> Yes <input type="checkbox"/> No            |

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

(APPLICATION NUMBER)

(FILING DATE)

(APPLICATION NUMBER)

(FILING DATE)

**COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D)**  
(Includes Reference to Provisional and International (PCT) Applications)

Attorney's Docket  
No. 032326-072

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or International (PCT) Application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability as defined in Title 37, Code of Federal Regulations § 1.56, which became available between the filing date of the prior application(s) and the national or international filing date of this application:

PRIOR U.S. APPLICATIONS OR INTERNATIONAL (PCT) APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120:

| U.S. APPLICATIONS                     |                  | STATUS (check one)                         |                          |                          |
|---------------------------------------|------------------|--------------------------------------------|--------------------------|--------------------------|
| U.S. APPLICATION NUMBER               | U.S. FILING DATE | PATENTED                                   | PENDING                  | ABANDONED                |
|                                       |                  | <input type="checkbox"/>                   | <input type="checkbox"/> | <input type="checkbox"/> |
|                                       |                  |                                            |                          |                          |
|                                       |                  |                                            |                          |                          |
| PCT APPLICATIONS DESIGNATING THE U.S. |                  |                                            |                          |                          |
| PCT APPLICATION NO.                   | PCT FILING DATE  | U.S. APPLICATION NUMBERS ASSIGNED (if any) |                          |                          |
| PCT/FR99/00583                        | 16 March 1999    |                                            |                          |                          |
|                                       |                  |                                            |                          |                          |
|                                       |                  |                                            |                          |                          |
|                                       |                  |                                            |                          |                          |

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the U.S. Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

|                          |        |                         |        |                        |        |
|--------------------------|--------|-------------------------|--------|------------------------|--------|
| William L. Mathis        | 17,337 | R. Danny Huntington     | 27,903 | Gerald F. Swias        | 30,113 |
| Robert S. Swecker        | 19,885 | Eric H. Weisblatt       | 30,505 | Charles F. Wieland III | 33,096 |
| Platon N. Mandros        | 22,124 | James W. Peterson       | 26,057 | Bruce T. Wieder        | 33,815 |
| Benton S. Duffett, Jr.   | 22,030 | Teresa Stanek Rea       | 30,427 | Todd R. Walters        | 34,040 |
| Norman H. Stepien        | 22,716 | Robert E. Krebs         | 25,885 | Ronni S. Jilions       | 31,979 |
| Ronald L. Grudziecki     | 24,970 | William C. Rowland      | 30,888 | Harold R. Brown III    | 36,341 |
| Fredrick G. Michaud, Jr. | 26,003 | T. Gene Dillahunty      | 25,423 | Allen R. Baum          | 36,086 |
| Alan E. Kopecki          | 25,813 | Patrick C. Keane        | 32,858 | Steven M. duBois       | 35,023 |
| Regis E. Slutter         | 26,999 | B. Jefferson Boggs, Jr. | 32,344 | Brian P. O'Shaughnessy | 32,747 |
| Samuel C. Miller, III    | 27,360 | William H. Benz         | 25,952 | Kenneth B. Lefler      | 36,075 |
| Robert G. Mukai          | 28,531 | Peter K. Skiff          | 31,917 | Fred W. Hathaway       | 32,236 |
| George A. Hovanec, Jr.   | 28,223 | Richard J. McGrath      | 29,195 |                        |        |
| James A. LaBarre         | 28,632 | Matthew L. Schneider    | 32,814 |                        |        |
| E. Joseph Gess           | 28,510 | Michael G. Savage       | 32,596 |                        |        |



and: \_\_\_\_\_

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

|                                                                                                                                                               |  |                                     |                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-------------------------------------|---------------------------|
| <b>COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D)</b><br>(Includes Reference to Provisional and International (PCT) Applications) |  | Attorney's Docket No.<br>032326-072 |                           |
| FULL NAME OF SOLE OR FIRST INVENTOR<br><i>Nathalie FEYT</i>                                                                                                   |  | SIGNATURE<br><i>[Signature]</i>     | DATE<br><i>30/10/2000</i> |
| RESIDENCE (CITY & STATE/COUNTRY)<br>Bt 6 - 20 rue du Lieutenant J.P. Meschi, 13005 <i>Marseille</i> , FRANCE <i>FR</i>                                        |  | CITIZENSHIP<br>France               |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)<br>Bt 6 - 20 rue du Lieutenant J.P. Meschi, 13005 Marseille, FRANCE                                                        |  |                                     |                           |
| FULL NAME OF SECOND JOINT INVENTOR, IF ANY<br><i>Olivier BENOIT</i>                                                                                           |  | SIGNATURE<br><i>[Signature]</i>     | DATE<br><i>08/10/2000</i> |
| RESIDENCE (CITY & STATE/COUNTRY)<br>22 rue Rasteguc, 13400 <i>Aubagne</i> , FRANCE <i>FR</i>                                                                  |  | CITIZENSHIP<br>France               |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)<br>22 rue Rasteguc, 13400 Aubagne, FRANCE                                                                                  |  |                                     |                           |
| FULL NAME OF THIRD JOINT INVENTOR, IF ANY<br><i>David NACCACHE</i>                                                                                            |  | SIGNATURE<br><i>[Signature]</i>     | DATE<br><i>11/11/2000</i> |
| RESIDENCE (CITY & STATE/COUNTRY)<br>7, rue Chapital, 75009, <i>Paris</i> , FRANCE <i>FR</i>                                                                   |  | CITIZENSHIP<br>France               |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)<br>7, rue Chapital, 75009, Paris, FRANCE                                                                                   |  |                                     |                           |
| FULL NAME OF FOURTH JOINT INVENTOR, IF ANY                                                                                                                    |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |
| FULL NAME OF FIFTH JOINT INVENTOR, IF ANY                                                                                                                     |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |
| FULL NAME OF SIXTH JOINT INVENTOR, IF ANY                                                                                                                     |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |
| FULL NAME OF SEVENTH JOINT INVENTOR, IF ANY                                                                                                                   |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |
| FULL NAME OF EIGHTH JOINT INVENTOR, IF ANY                                                                                                                    |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |
| FULL NAME OF NINTH JOINT INVENTOR, IF ANY                                                                                                                     |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |
| FULL NAME OF TENTH JOINT INVENTOR, IF ANY                                                                                                                     |  | SIGNATURE                           | DATE                      |
| RESIDENCE (CITY & STATE/COUNTRY)                                                                                                                              |  | CITIZENSHIP                         |                           |
| POST OFFICE ADDRESS (HOME ADDRESS)                                                                                                                            |  |                                     |                           |